High-Resolution ADC Using Delta-Sigma Architectures

DESIGN DOCUMENT

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1.4 List of Symbols

Id	Diode Current
Iss	Diode Reverse Saturation Current
Vd	Voltage Across a Diode
Vt	Thermal Voltage
K	Boltzmann's Constant
T	Temperature
q	Electron Charge

n **Number of Diodes**

1.5 List of Definitions

Integrated circuit (IC) – an electronic circuit formed on a piece of semiconducting material.[1]

Analog to digital converter (ADC) – an electronic device that converts an analog signal to a digital signal without altering its essential content.[2]

Throttle – control the operation speed of a circuit, and therefore its heat dissipation rate.

Sample – reduce a continuous-time signal to a discrete-time signal by collecting a series of its values at regularly spaced intervals.[3]

Resolution – the number of discrete output values an ADC can produce over the range of analog input values.[4]

Delta-sigma ADC – an ADC that produces a high-resolution output signal using oversampling techniques.[5]

DAC – an electronic device that converts a digital signal to an analog signal without altering its essential content.[6]

Modulator – an electronic device that varies one or more properties of a periodic waveform.[7]

Digital Filter – a system that performs mathematical operations on a discrete-time signal to modify certain aspects of that signal.[8]

Digital Decimator – a device that reduces the sampling rate of a digital signal.[9]

Parasitic Capacitance – a usually unwanted capacitance that exists between parts of electronic components or circuits because of their proximity to each other.[10]

Switched Capacitor Integrator – an electronic device that performs an integrating function using an operational amplifier and a switch-connected capacitor that acts as a current-limiting component.

Comparator – an electronic circuit that compares two voltages and outputs a digital signal indicating which voltage is larger.[11]

Layout – a representation of an integrated circuit using geometric shapes that correspond to the patterns of the materials that make up the physical integrated circuit.[12]

2 Introductory Material

2.1 Acknowledgement

The development of this design is supported by faculty advisor Dr. Randall Geiger. We would like to thank Dr. Geiger for providing the key insight and expertise that greatly assists our project. His contributions are crucial in ensuring that our team fully comprehends the necessary technical material for this project.

2.2 Problem Statement

We rely heavily on various integrated circuits (IC) to perform as intended every day. Without these circuits, we would have a difficult time with typical day to day tasks. Heat can become a serious issue with ICs. When these chips overheat, it can damage the circuit and cause it to malfunction. There is a need for a method to measure and communicate the chip temperature to circuitry that will throttle the circuit activity when necessary.

Our team has proposed to design a temperature sensor and a delta-sigma analog-to-digital converter (ADC) to convert the temperature sensor's output to a digital signal. This circuit will accurately measure, and communicate in a digital format, the temperature of the IC. With this technology, the temperature of an IC can be monitored and controlled as it is being used to ensure that it doesn't overheat.

2.3 Operating Environment

Our circuit can be integrated with any IC as it is intended to monitor the temperature of that IC. The operating environment will vary depending on the system the circuit is integrated with. For most purposes, this will result in the circuit being used in a small enclosed environment.

2.4 Intended Users and Intended Uses

Our product is to be used by IC designers when designing new ICs. They will integrate our circuit with the IC they are designing. The circuit is intended to be used by IC designers in both industry and in academic research.

Our product will be used to measure and communicate the temperature of an IC to other parts of the IC responsible for temperature control. Based on the output of our circuit, the connected circuitry will change the IC's rate of activity to reduce heat dissipation when the temperature rises above a certain threshold.

2.5 Assumptions and Limitations

Assumptions:

- The temperature of the IC in which the temperature sensor and ADC are used will remain between 10 degrees and 60 degrees Celsius.
- Two accurate reference voltages of 765 millivolts (Vref) and 800 millivolts (Vref+) will be provided to the ADC.

Limitations:

- The area of the physical layout of the circuit is no more than 4 millimeters by 4 millimeters.
- The supply voltage is 0V to 1.8V

2.6 Expected End Product and Other Deliverables

The ADC will be a fabricated IC containing our ADC and temperature sensor. It will be fabricated through MOSIS over the summer of 2018. The fabrication will be completed by August 2018 to allow our team to test for functionality of the IC during the Fall 2018 semester.

We will also produce an assessment of the performance capabilities and limitations of over-sampled data converters, testing results for our complete circuit, and an assessment of the overall performance of the ADC and the temperature sensor based upon the experimental results and their relation to the simulation results.

3 Specifications and Analysis

3.1 Specifications

The specifications that this project is designed to meet are the following:

- The circuit should be designed in the 0.18 um TSMC CMOS process.
- The area of the physical layout is to be no more than 4 millimeters by 4 millimeters.
- The ADC should output at least 1 output code per 10 milliseconds.
- The ADC should have a targeted resolution of 10 bits.
- The temperature sensor should have a monotonic relationship between temperature and output voltage.
- The temperature sensor and ADC system should be able to measure temperatures in the 10-degree to 60-degree Celsius range.

3.2 Approach

There are a large variety of data converter architectures that are currently available. This project specifically asked for the design of a delta-sigma data converter although other designs considered were a SAR and Nyquist rate data converter. The SAR (Successive-approximation) data converter is one of the oldest and most common data converter architectures. The SAR is used when there are multiple inputs, and it is mainly implemented in industrial control applications. The Nyquist data converters are data converters sampled at the Nyquist rate frequency. These data converters cannot reach a high resolution and experience a higher level of quantization noise at the output.

The chosen design, the Delta Sigma ADC, has characteristics that make it the best fit for our application of measuring the voltage output of a temperature sensor. The delta-sigma ADC experiences a low level of

quantization noise at the output. This is achieved through oversampling of the input signal. The Delta Sigma architecture produces a high-resolution output, which will provide an accurate temperature reading from our sensor. Our delta-sigma ADC design is based on the design in the textbook *Analog Integrated Circuit Design*[13]. We modified the design to use first-order modulator and decimator circuits instead of higher-order circuits. The strengths of the first-order circuit are that it is sufficient for providing the desired output, makes the circuit easier to design and build in the short time we have, and allows for a circuit with a very small die footprint. A weakness in choosing this simpler design is that the first-order circuit will not carry out noise shaping in the ADC which would result in a more accurate output and is exemplified in the *IEEE Journal of Solid-State Circuits* article, "A 43-mW MASH 2-2 CT ΣΔ Modulator Attaining 74.4/75.8/76.8 dB of SNDR/SNR/DR and 50 MHz of BW in 40-nm CMOS."[14]

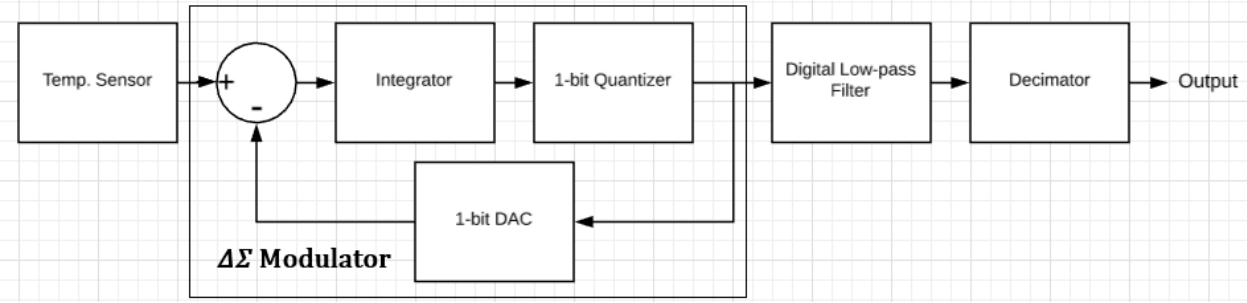

Figure 3.2.1: Delta-Sigma ADC Block Diagram

Our approach for this project is to implement an integrated circuit consisting of a temperature sensor and delta-sigma ADC using the top-level architecture shown in Figure 3.1. The design consists of a temperature sensor, a delta-sigma modulator, and a digital filter/decimator. The ADC is designed to take samples of the temperature sensor output at a rate of 102.4 kHz and output a 10-bit binary representation of the temperature at a data rate of 100 Hz.

3.3 Temperature Sensor

Temperature is a physical quantity that can be identified as a low frequency analog signal. For example, the temperature in a room will not change a few degrees in a matter of one or two milliseconds. To measure temperature the sensor needed to be designed using a temperature dependent device. The design used in this project implemented diodes as the temperature dependent devices. The equation for the current through a diode is given in as[15]:

$$Id = Iss * (e^{Vd/Vt} - 1) \quad . \tag{3.3.1}$$

Id = current across the diode
Iss = reverse saturation current
Vd= diode voltage
VT = Thermal Voltage

Fixing the current across the diode will allow the voltage across the diode to change as the thermal voltage changes. The design of the temperature sensor is shown below, this circuit produces a linear and accurate output.[16]

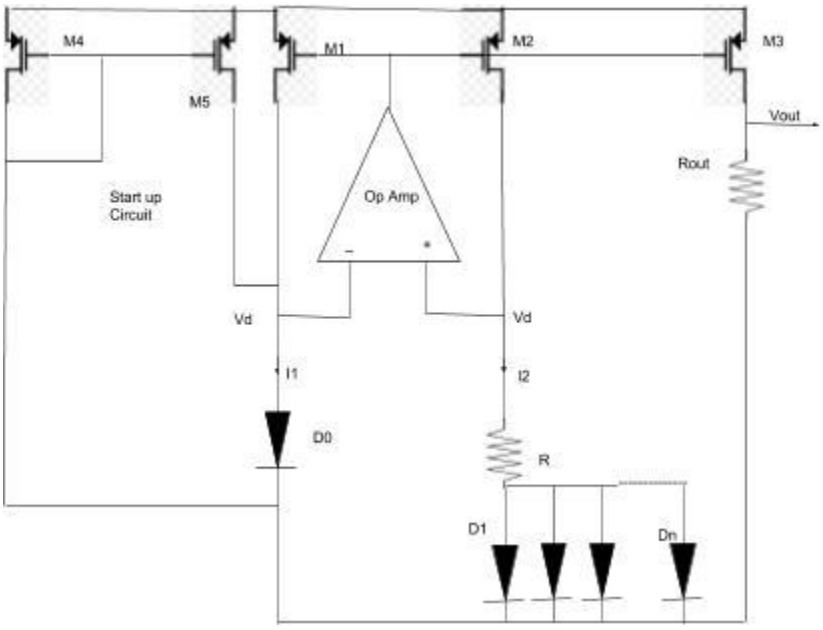

Figure 3.3.1: Temperature Sensor Structure

The output of the circuit is given by the following equation:

$$\text{Vout} = \frac{KT}{q} * \frac{R_{out}}{R} * \ln(n) \quad . \tag{3.3.2}$$

K= Boltzmann's constant
T=temperature
q= electron charge
n= number of diodes

A diode can simply be implemented using a diode-connected transistor, where the gate of the transistor is connected to its drain. The operational amplifier used in this design is a single-stage telescopic cascode operational amplifier.

A Cadence schematic of our temperature sensor design is shown in Figure 3.3.2.

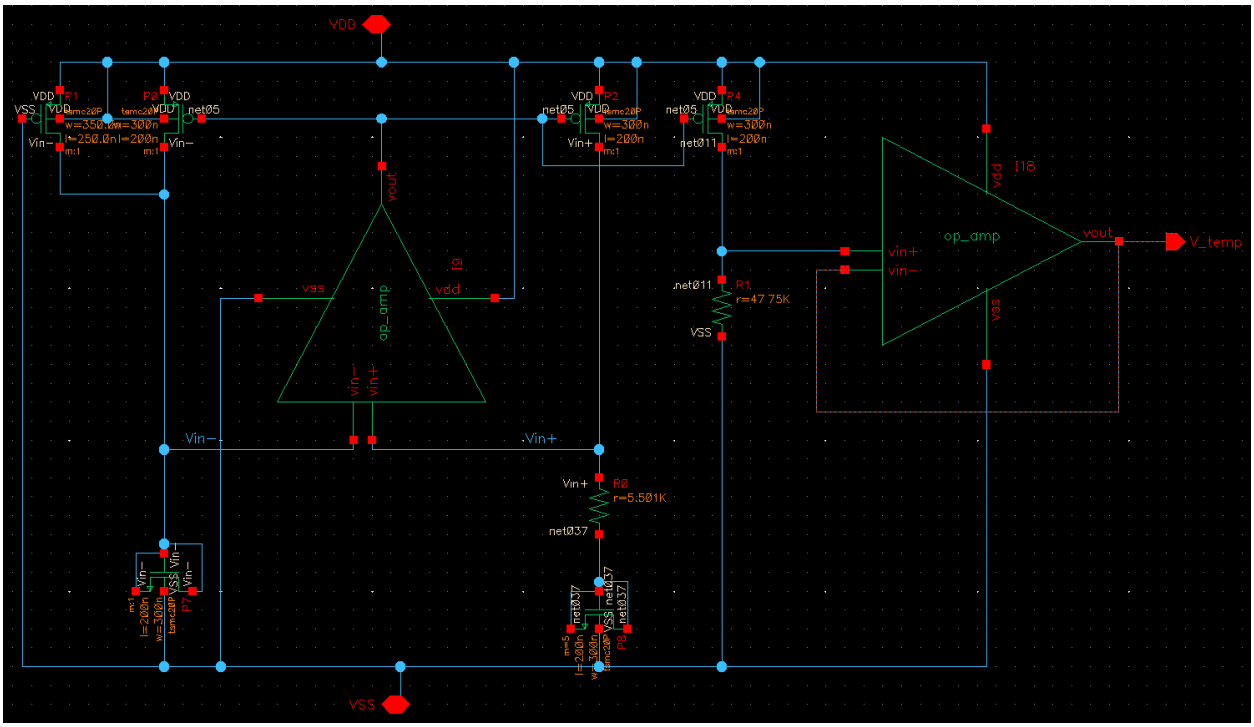

Figure 3.3.2: Temperature Sensor Schematic

3.4 CLOCK

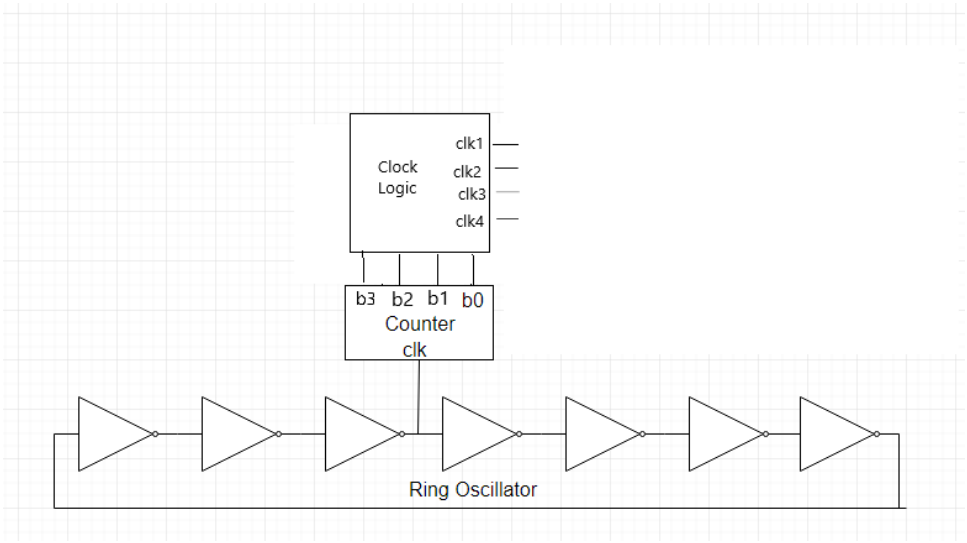

Figure 3,4.1: Clock Generating Circuit

A ring oscillator, which consists of a ring of 23 inverters, generates the main clock, which has a frequency of 1638.4 kHz. This is converted to clk1, clk2, clk3, and clk4 with counter and logic circuits. The frequency of the resulting 4 clock signals is 102.4 kHz. The clock circuit diagram is shown in Figure 3.4.1. Figure 3.4.2

shows the schematic of the clock logic. The Reg_DFF blocks are flip flops used to latch the clock outputs to avoid unwanted spikes during high and low times.

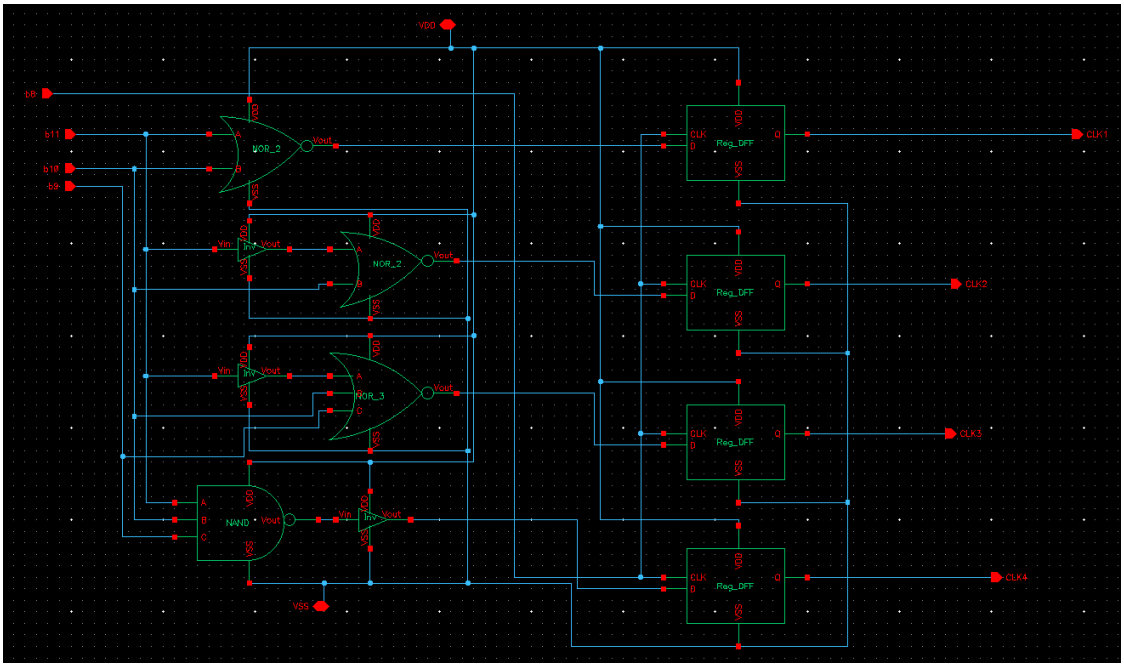

Figure 3,4.2: Clock Logic Schematic

The four resulting clock signals are shown in Figure 3.4.3.

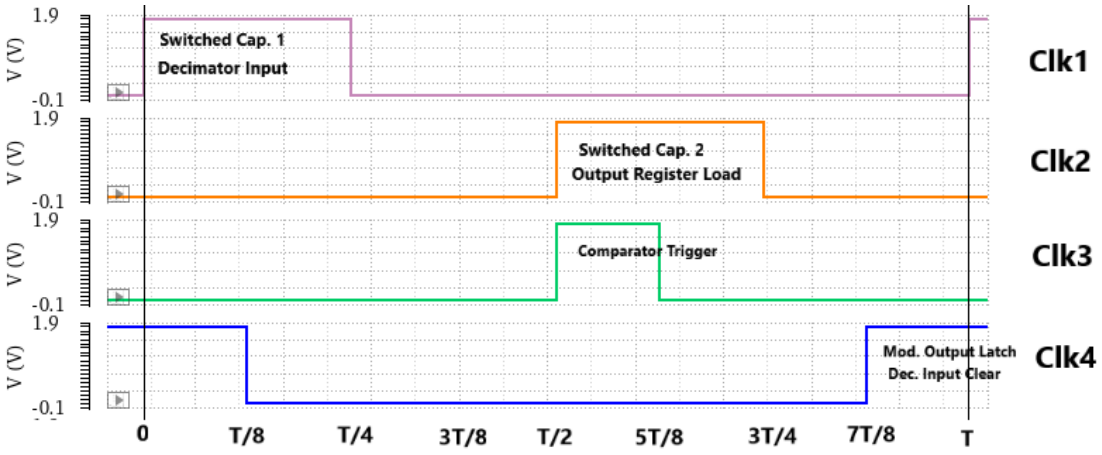

Figure 3,4.3: Clock Signal Diagram

3.5 Delta-Sigma Modulator

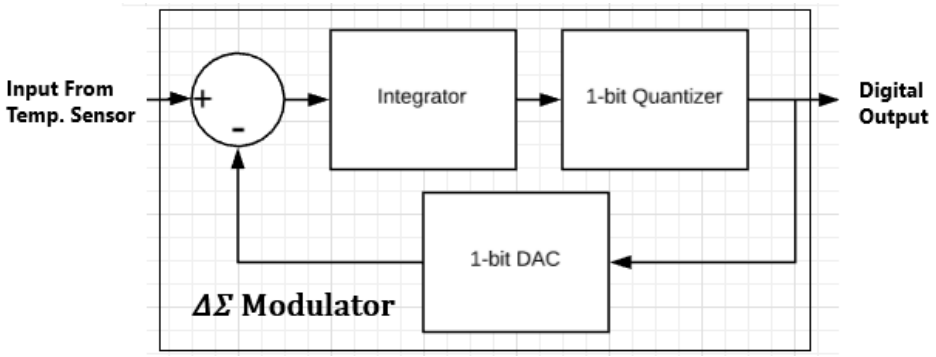

Figure 3.5.1: Block Diagram of Delta-Sigma Modulator

The delta-sigma modulator is the first of the two main parts of the delta-sigma ADC. The modulator takes the analog output of the temperature sensor as its input, and outputs a digital signal that contains the temperature data in the form of a data stream whose proportion of 1's to total values in a 10-millisecond time span is equal to the magnitude of the input voltage to the modulator relative to the input voltage range. The modulator contains three main functional blocks: an integrator, a 1-bit quantizer (a comparator), and a 1-bit DAC. The Cadence schematic of our modulator is shown in Figure 3.5.2.

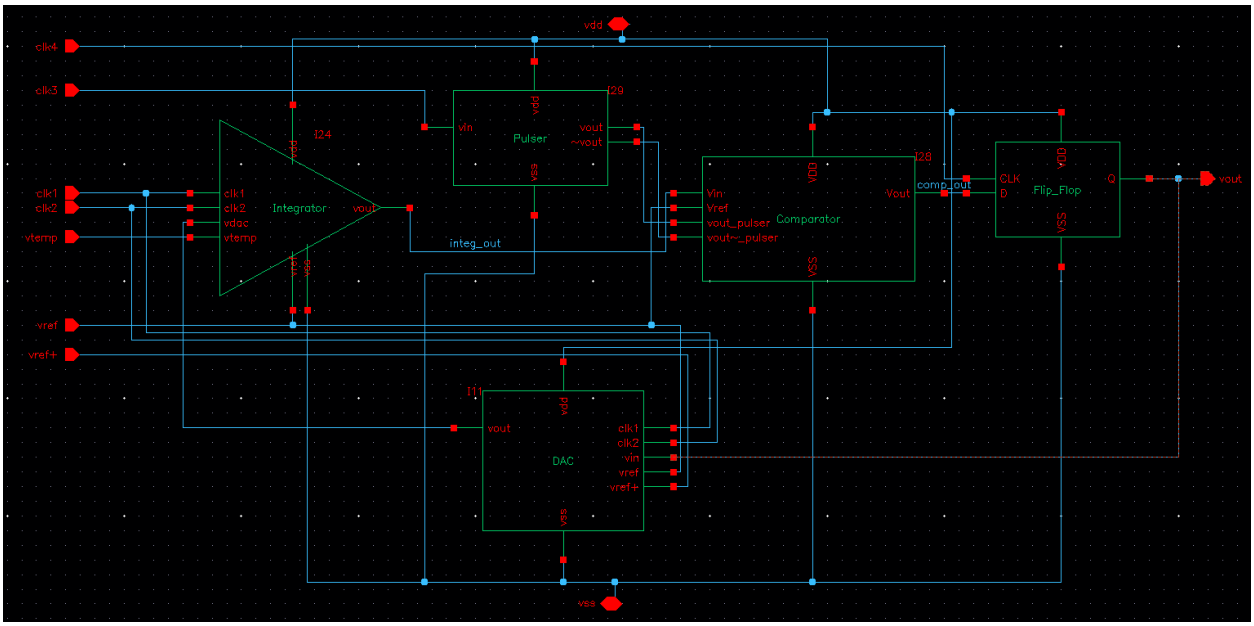

Figure 3.5.2: Schematic of Delta-Sigma Modulator

3.5.1 INTEGRATOR

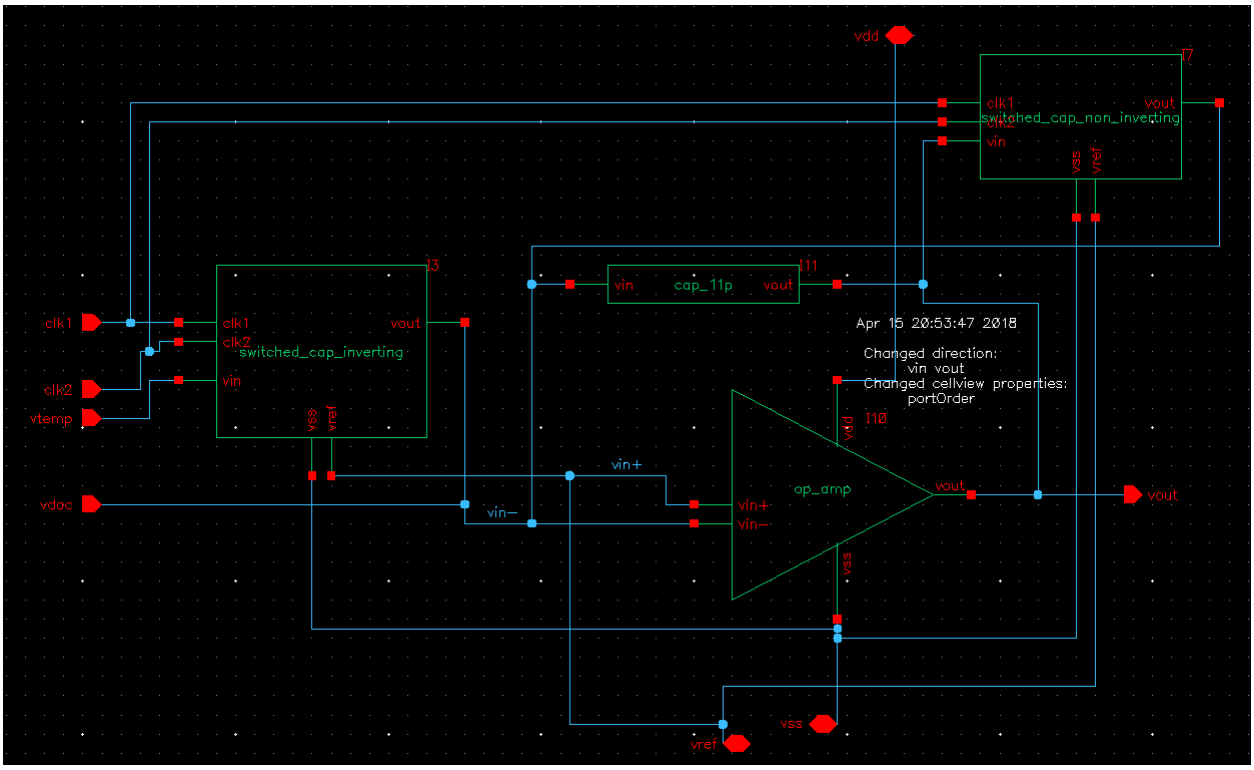

Figure 3.5.1.1: Integrator

The integrator is the functional block that generates a sawtooth wave that acts as the input to the comparator. The voltage output of the integrator progresses in a negative or positive direction depending on the sign of the input voltage.[5] The slope of this progression depends on the magnitude of the input voltage. The integrator consists of an op amp with a feedback capacitor, a feedback switched-capacitor, and a switched-capacitor input. The input switched capacitor input acts as a resistance for the ADC input. The feedback capacitor performs the integrating function by accumulating charge. The feedback switched capacitor acts as a resistor that prevents error from accumulating on the output due to charge accumulating on the feedback capacitor from offset voltage.

The output of the integrator is a saw-tooth wave. The proportion of the time that this wave is above the comparator's switching voltage (768.5mV) is proportional to the magnitude of the input voltage to the ADC relative to the input voltage range (730mV to 800mV). The integrator outputs with a range of input voltages applied are shown in Figure 3.5.1.2. Input voltages are expressed as a percentage of the input voltage range at the left side of the figure. The black lines are the comparator switching voltage.

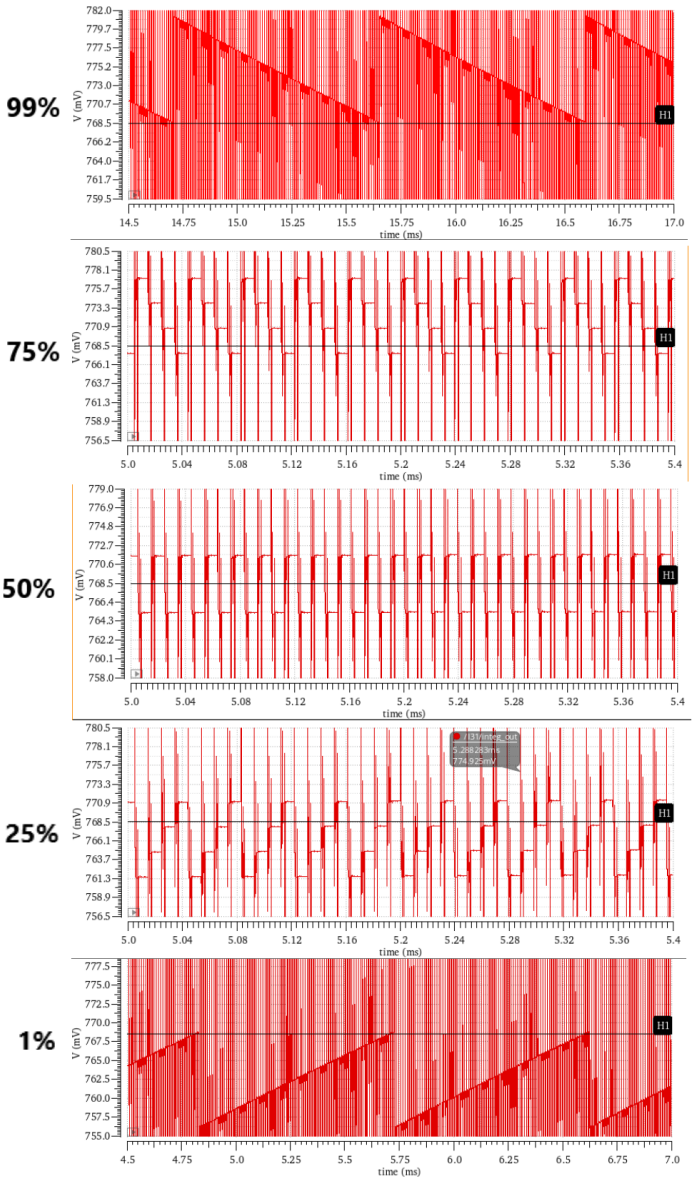

Figure 3.5.1.2: Integrator Outputs with Various Input Voltages Applied

3.5.2 SWITCHED CAPACITOR

The switched capacitor circuits each consist of a capacitor and four switches. The circuit can be made to be either inverting or non-inverting by simply changing the clocking of the switches. Clock 1 and Clock 2 are 180-degrees out of phase and have 25% percent duty cycles to ensure that they do not overlap, which would cause a short circuit. Schematics of both types of switched capacitor circuits are given in Figures 3.5.2.1 and 3.5.2.2.

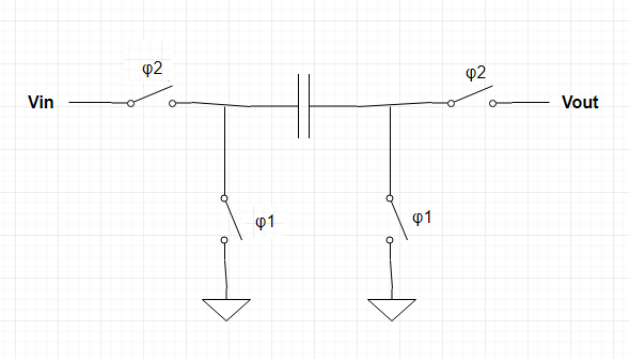

Figure 3.5.2.1: Non-Inverting Switched Capacitor Circuit

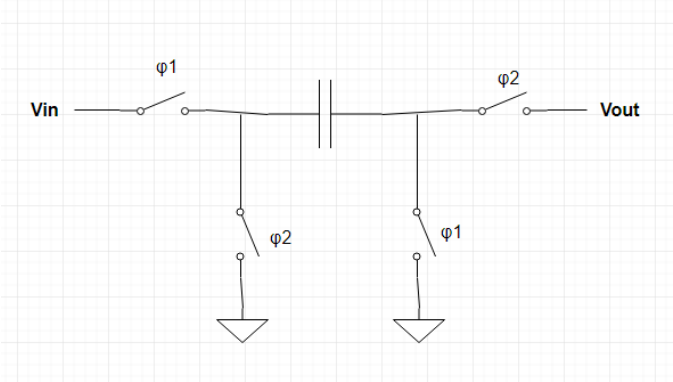

Figure 3.5.2.2: Inverting Switched Capacitor Circuit

The switched capacitor circuits act as resistors by restricting the flow of charge through them. The effective resistance is given by:

$$R_{EFF} = \frac{1}{C * f_{CLOCK}}. \tag{3.5.2}$$

Using a switched capacitor circuit allows a large resistance to be provided without the large die space consumption of a resistor.

3.5.3 Operational Amplifier

The operational amplifier used in our integrator has a single-stage telescopic cascode architecture (Figure 3.5.3.1)

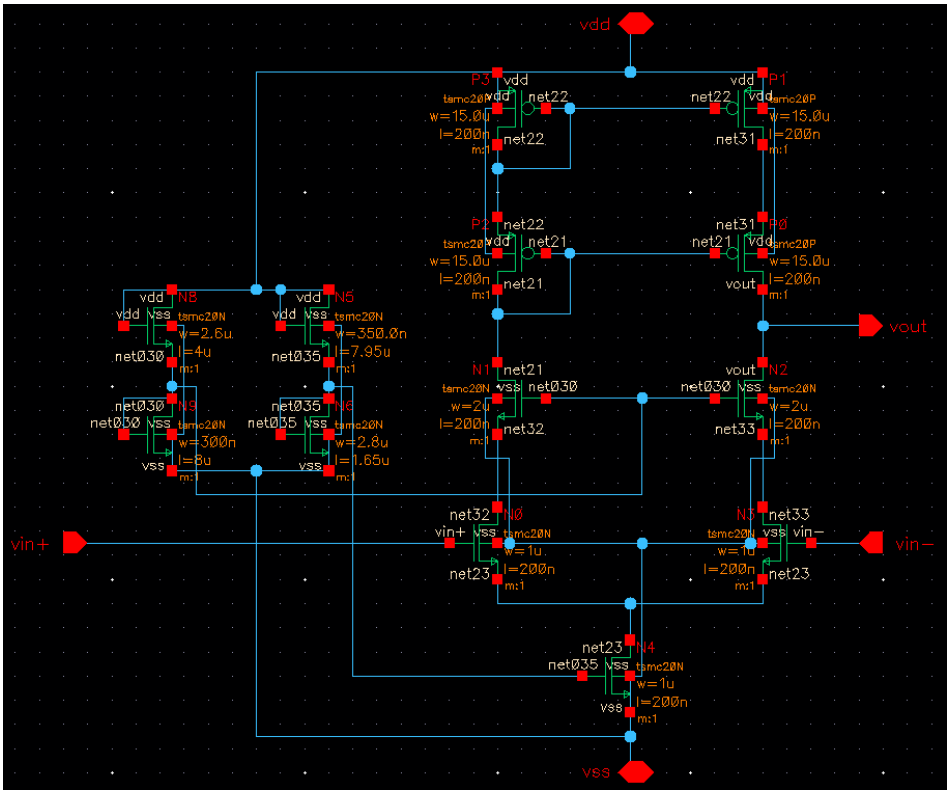

Figure 3.5.3.1: Telescopic Cascode Op Amp

Using this architecture allows for a high gain (~70dB) without the necessity of a second stage. This avoids the need for a feedback capacitor which would take up a large amount of die space.

3.5.4 Comparator

A 1-bit ADC reads in a voltage and produces a 1-bit digital output, such as 1 or 0. A comparator reads in a voltage and compares it to a voltage reference and outputs VDD or VSS, which are interpreted as a 1 or 0. A dynamic comparator only produces an output at a clock edge. The dynamic comparator uses strong positive feedback for a regeneration phase when a clock is high and passes through a reset phase when the clock is low.

The dynamic comparator that was used in the Delta Sigma data converter is shown in Figure 3.5.4.1.

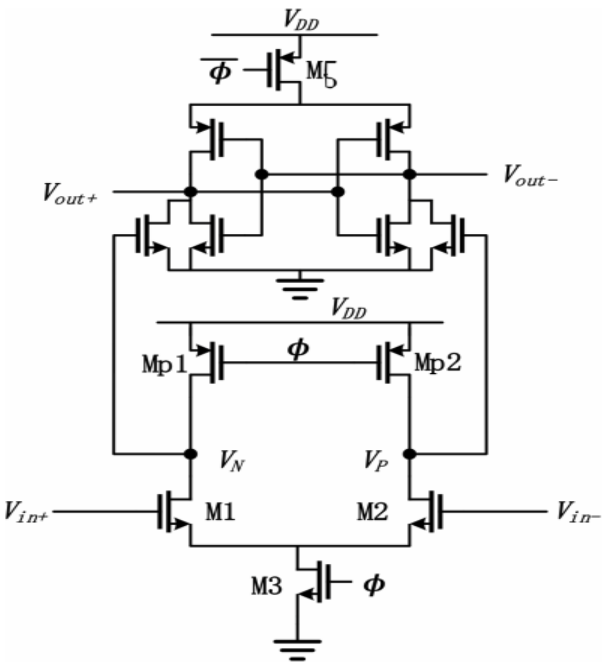

Figure 3.5.4.1: Dynamic Comparator

Functionality of the Dynamic comparator:

The dynamic comparator shown above is a conventional double tail comparator with a preamplifier[1]. This dynamic comparator will amplify a small voltage signal difference between V_{in} and V_{in-} allowing the latch to function accurately. When the clock ϕ goes low both the PMOS and NMOS tail transistors turn off and the nodes V_N and V_P have voltages at VDD. The tail transistors turning off also will avoid static power dissipation. When the clock ϕ goes high the voltages at the output will be discharged by the bottom transistors M1, M2, and M3. The nodes V_N and V_P will begin to drop and different rates due to the input voltages and transistors M1 and M2. If M1 has a larger input voltage than M2 the voltage at V_N will drop faster than the voltage at V_P. This will cause a smaller gate to source voltage on transistor M4 than M5, and a smaller current at V_{out+} than V_{out-}. The regenerative latch acts like an SR latch and pulls one output high and one low. Essentially if V_{in} is larger than V_{ref} it pulls V_{out} to VDD and V_{out-} to VSS, if V_{in} is smaller than V_{ref} it pulls V_{out} to VSS and V_{out-} to VDD, if V_{in} is equal to V_{ref} it will enter a metastable state and produce one of the previously stated outputs.[17]

Shown below is the timing diagram of ϕ and $\bar{\phi}$ and the voltages at nodes V_N and $V_{P;}$ it is shown that when ϕ is low V_N and V_P are at VDD and they begin to discharge when ϕ is high.

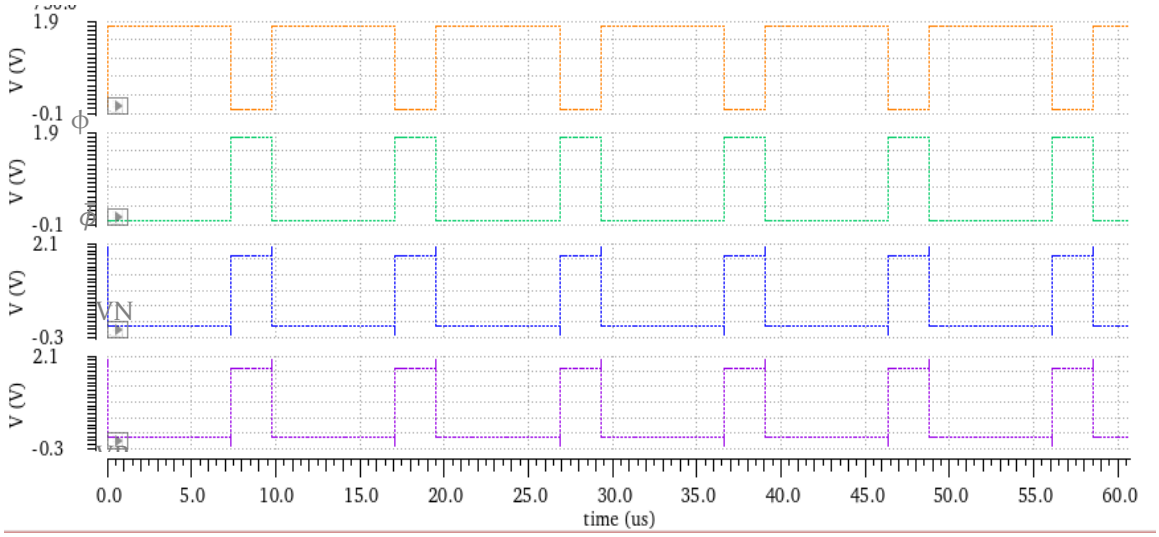

Figure 3.5.4.2: Comparator Clocking

Shown below is the timing diagram of ϕ, $\bar{\phi}$, V_{in}, V_{ref}, and V_{out}. It is shown that the output will not compare the input voltage and the reference voltage until it is at a clock edge. The first line shows where V_{in} surpasses V_{ref} and the second line shows where the clock edge occurs, and V_{out} goes high.

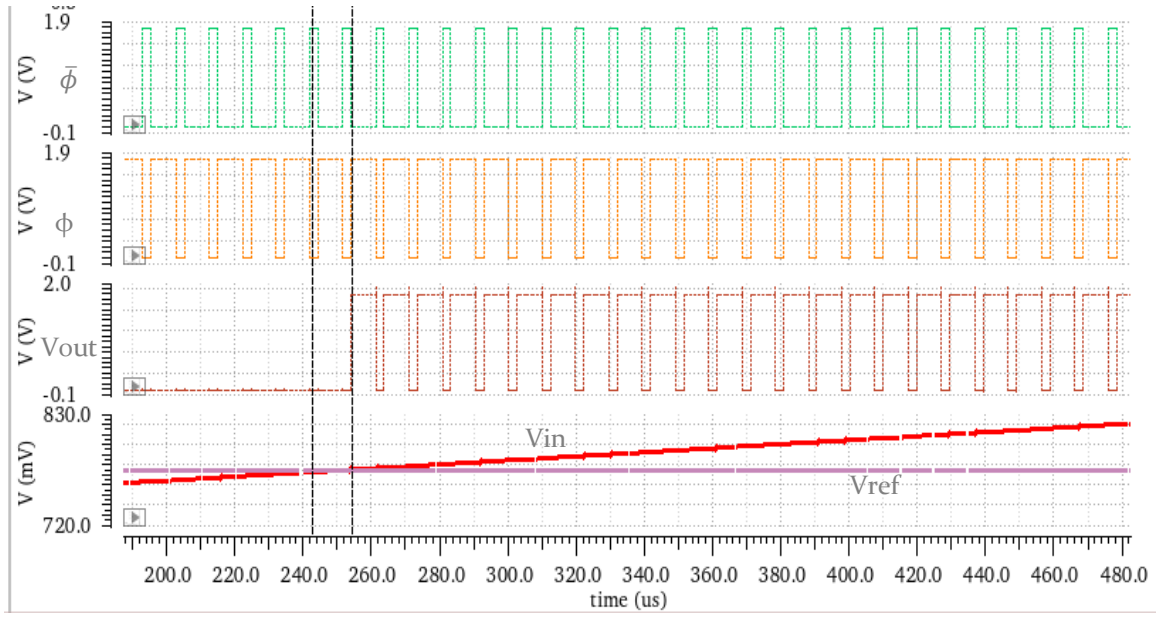

Figure 3.5.4.3: Dynamic Comparator Timing Diagram

The output of the comparator acts as the output of the delta-sigma modulator. The comparator's output is shown for several modulator input voltages in the input voltage range. Input voltages are expressed as a percentage of the input voltage range at the left side of the figure.

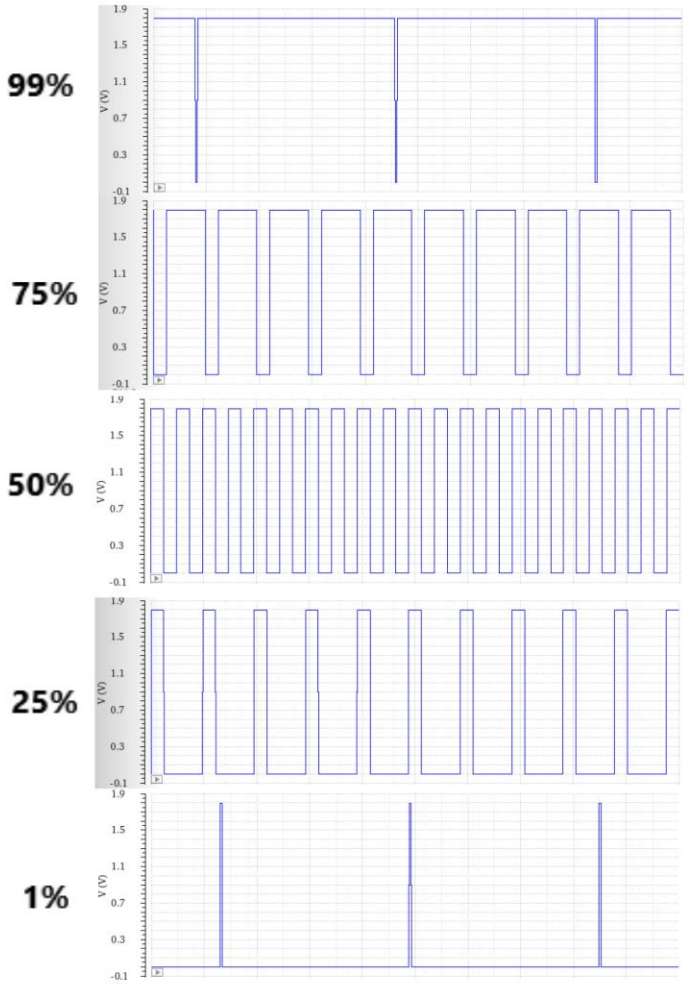

Figure 3.5.4.4: Comparator Outputs with a Range of Input Voltages Applied to ADC

The schematic of our comparator is shown in Figure 3.5.4.5

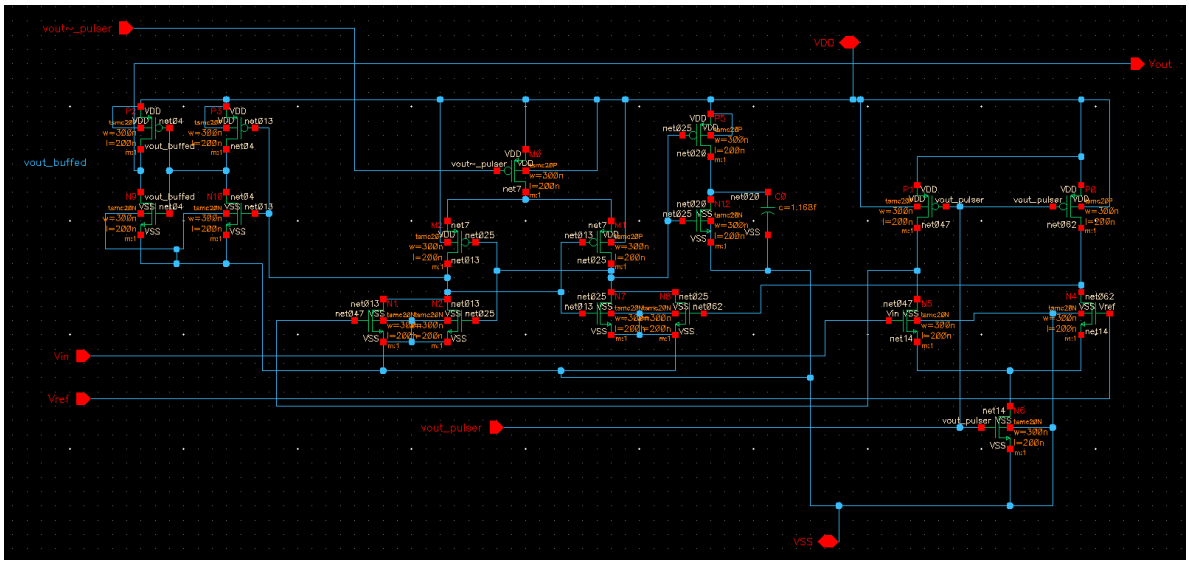

Figure 3.5.4.4: Comparator Schematic

3.5.5 DAC

The 1-bit digital-to-analog converter (DAC) functions to take a digital input from the output of the comparator and convert it into an analog signal to be applied to the input of the integrator. This is accomplished using a switched capacitor with Vref+ connected to the input. By using the output of the comparator to control the clocking of the switched capacitor via two multiplexers, a positive or negative current is applied at the DAC's output depending on the output level of the comparator. By configuring the control switching appropriately, the modulator's differencing block is also implemented by the DAC. The DAC's circuit configuration is shown in the schematic in Figure 3.5.5.1

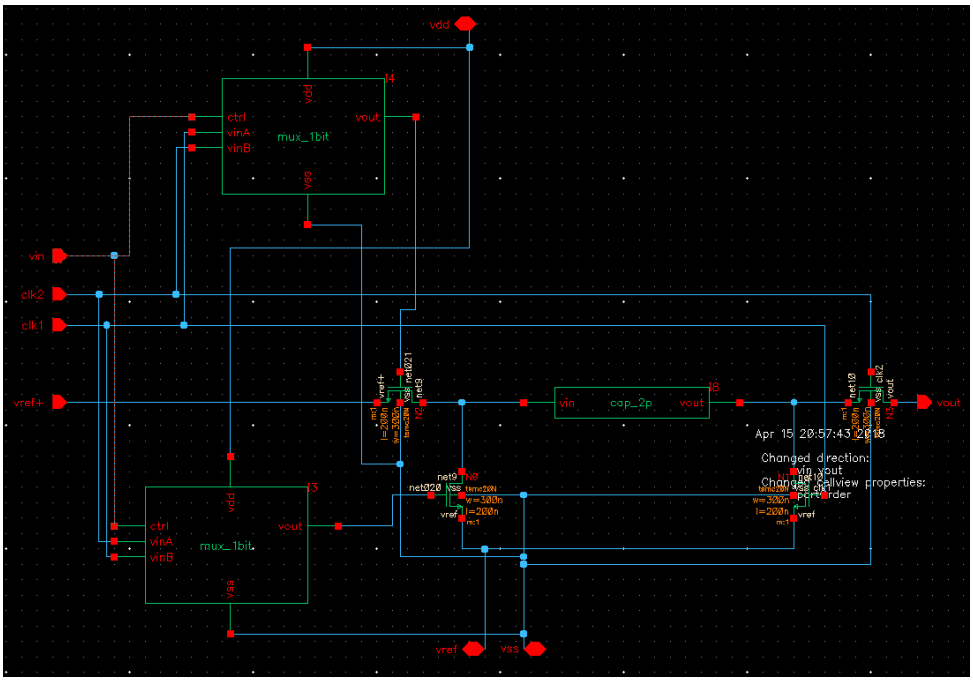

Figure 3.5.5.1: DAC Schematic

3.6 Digital Decimator

The digital portion of the delta-sigma ADC consists of a digital decimator. This block's function is to convert the binary data stream applied to its input by the modulator to a lower-frequency 10-bit parallel output. It accomplishes this by summing the inputs over 1024 clock cycle time spans and asserting these sums at its output. This results in a new output code every 10 milliseconds. The summing is accomplished by a 10-bit counter. The sum is then loaded to a 10-bit output register after every 1024 clock cycles, at which point the counter is reset. The loading of the register and resetting of the counter is controlled by another 10-bit counter which acts as a clock divider of the 102.4 kHz system clock. The schematic of this circuit is shown in Figure 3.6.1.

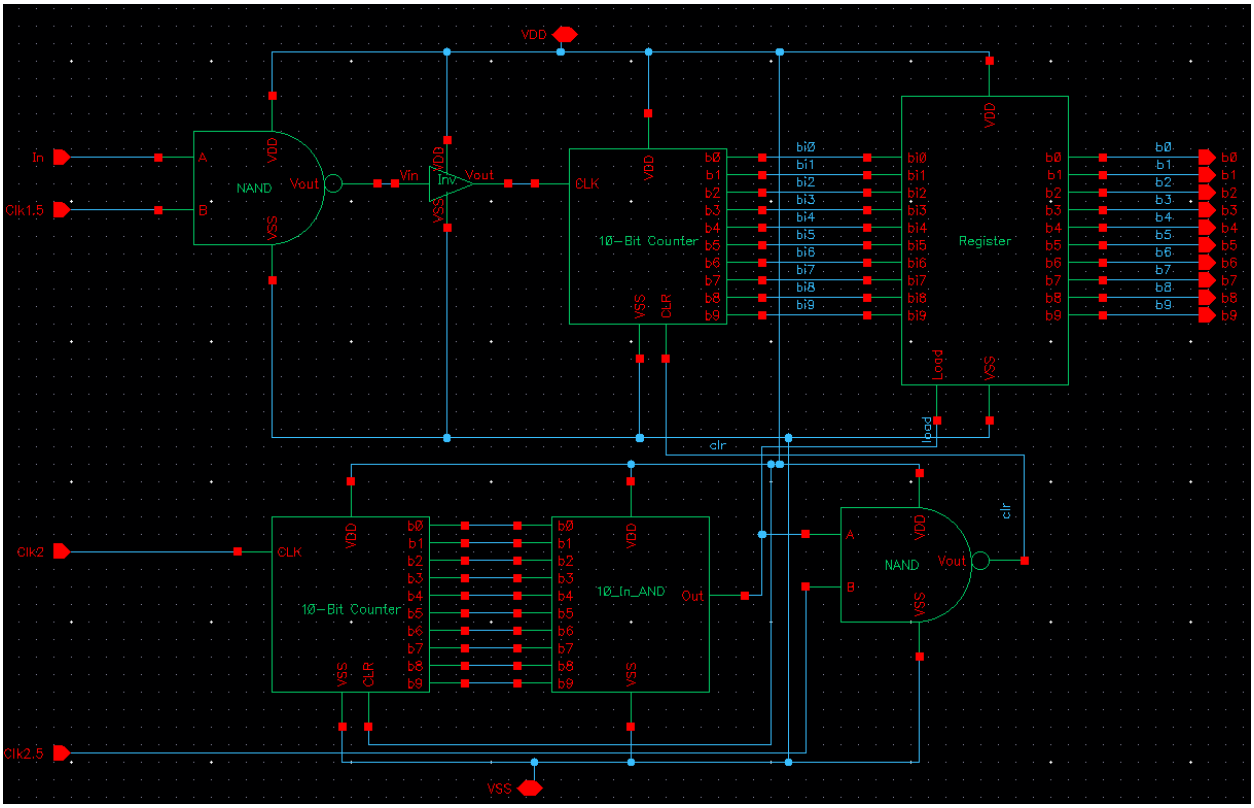

Figure 3.6.1: Decimator Schematic

The oversampling at the input of the modulator, followed by the 1024:1 decimation of the modulator's output signal, is what allows for the high accuracy of the delta-sigma ADC.

3.7 Physical Layout

Once we completed our circuit schematics, we used Cadence tools to create a physical layout of our circuit which will be used to specify how the circuit will be fabricated. Most of the area of the layout is taken up by the three large capacitors in our integrator circuit. However, since these were built using the Metal 5 and Metal 6 layers, this left many layers below to build the rest of our circuit layout. The full circuit layout with capacitors visibility removed is shown in Figure 3.7.1.

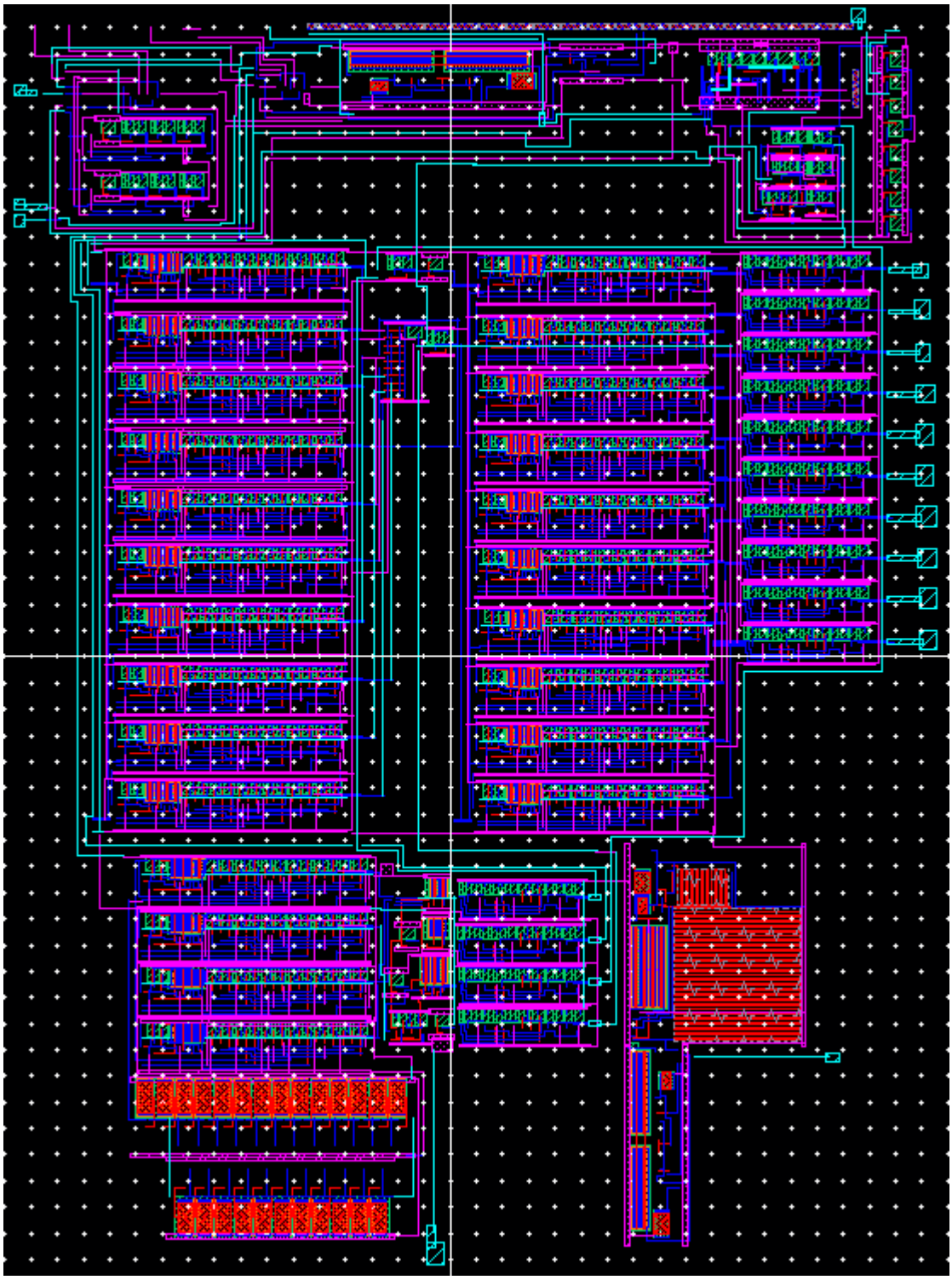

Figure 3.7.1: Circuit Physical Layout

The layout of the capacitors is shown in Figure 3.7.2.

Figure 3.7.2: Layout of Capacitors

3.8 Pad Frame

Having our circuit fabricated requires a pad frame. The pad frame provides pads where bonding wires can connect the package pins to our circuit's inputs and outputs. Another important feature of a pad frame is ESD protection circuitry. This circuitry consists of a diode and a resistor connected to each pad and serves to protect the circuit from electrostatic discharge through the IC pins. The pad frame that we will be using was created by Robert Buckley and Joseph Aymond, two ISU graduate students. The pad frame layout is shown in Figure 3.8.

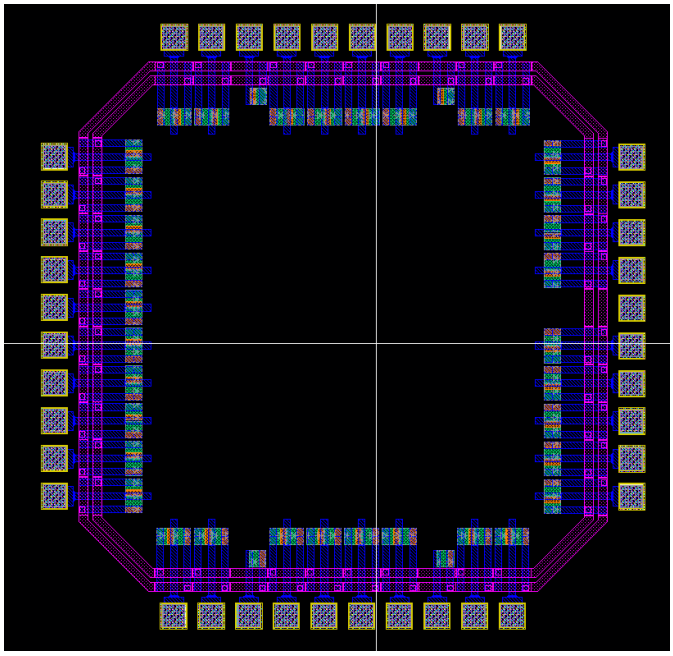

Figure 3.8: Pad Frame

3.9 Lack of Future Design Version

Since this is the final version of our project design, there will be no future version. Therefore, we have not distinguished between design details for present and future versions of the project.

4 Testing and Implementation

4.1 Interface Specifications

The input of the ADC should be a voltage in the range of 730mV to 800mV. Reference voltages of 756mV and 800mV should be connected to the appropriate pins. The output of the temperature sensor will be connected to a pin which can be connected to the ADC input pin for testing.

The output of the ADC will be a 10-bit parallel digital signal provided on 10 pins with 0V low voltage and 1.8V high voltage.

4.2 Pre-Fabrication Testing

The primary tool that we used for pre-fabrication testing of our ADC and temperature sensor is the Cadence ADE. This software tool is provided by the University for our use on the computers in Coover Hall. The Cadence ADE offers highly accurate design exploration, simulation, and verification for integrated circuits. Using this tool to run simulations allows us to ensure that our circuit will meet our requirements after it is fabricated.

4.2.1 TEMPERATURE SENSOR

The temperature sensor was tested using Cadence ADE. Simulations were done to verify the monotonicity of the relationship between temperature and output voltage, and to measure the output voltage range corresponding to the 10-degree to 60-degree Celsius temperature range.

The temperature sensor's functionality was tested by sweeping the temperature of the circuit across a range that included the 10 to 60-degree Celsius range of interest and plotting the output voltage. The results are shown in Figure 4.2.1.

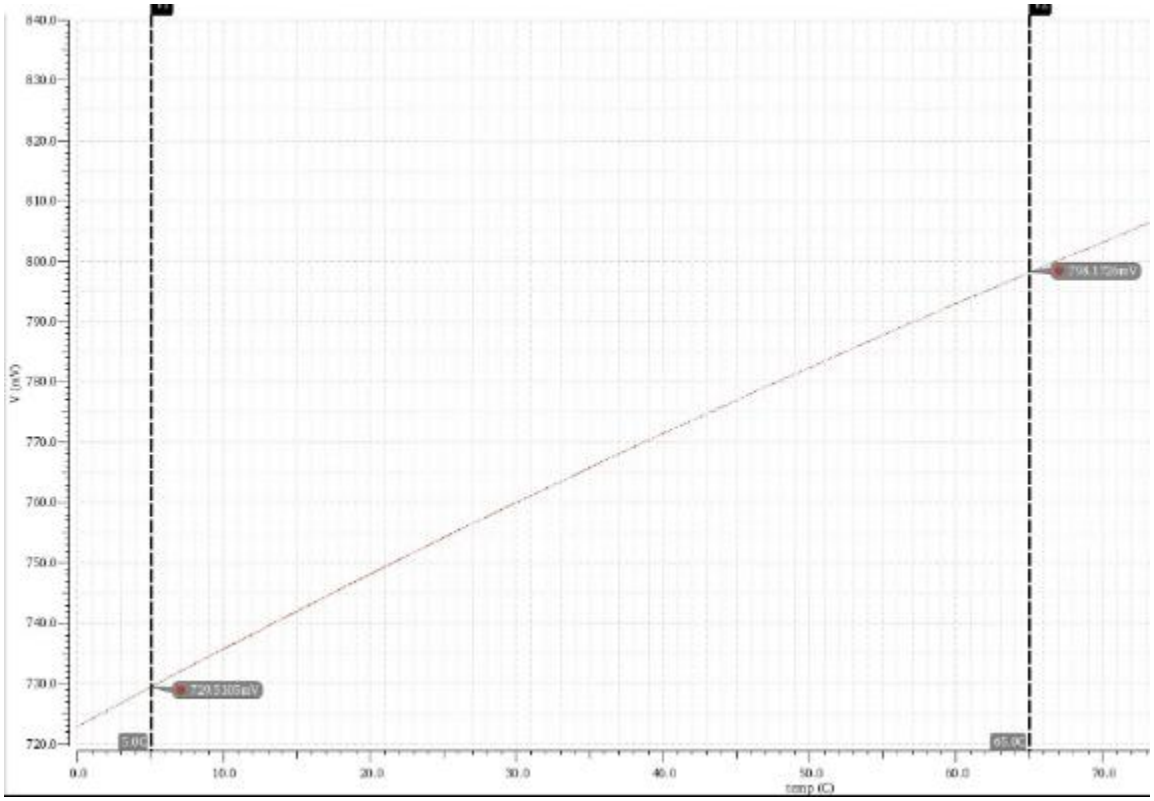

Figure 4.2.1: Temperature Sensor Output

These results verify that the temperature sensor has a monotonic output in the range of interest and operates as intended.

4.2.2 COMPARATOR

The comparator was tested using Cadence ADE. Simulations were done to verify the function of the circuit as a comparator, and the input signal swing. The proper input signal swing is necessary to insure the comparator circuit can react to the output of the integrator. The input signal swing range should include the 730mV to 800mV range and switching should occur near the center of this range.

We tested the comparator's functionality by applying a gradually increasing voltage to its input and plotting its output. We observed the input voltage, output voltage, and Vref (the trigger point) and saw that the output voltage change was triggered when the input voltage reached Vref as expected (Figure 4.2.2).

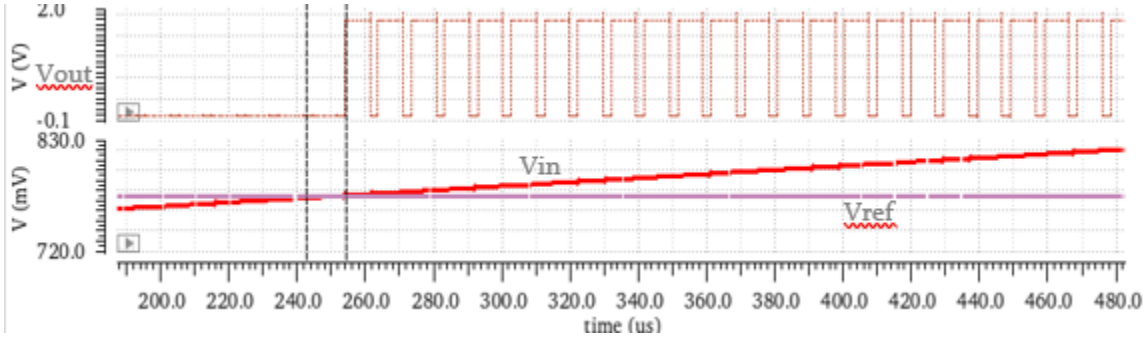

Figure 4.2.2: Comparator Test Results

This verified that the comparator's output voltage changed from low to high when Vin exceded Vref, as intended.

4.2.3 MODULATOR

The modulator was tested using Cadence ADE. Simulations were done to verify the functionality of the circuit. The behavior of the modulator should be that the proportion of the time that the output is high should be equal to the magnitude of the input voltage to the modulator relative to the input voltage range.

The modulator's functionality was tested by connecting the integrator, comparator, and DAC together in feedback configuration. The output of the modulator was then plotted with several input voltages applied to the modulator's input. An ideal flip flop was placed at the output to factor out voltage peaking. The plotted output was then integrated over a 100ms timespan to obtain a measure for what proportion of the time the output was high. This value was then compared to the expected value to obtain the error. The results of this testing are given in Table 4.2.3.

Table 4.2.3: Modulator Simulation Results

Input Voltage (mV)	Integrated Value (V*ms)	Expected Integrated Value (V*ms)	Error (%)	Error (V_{LSB})
731	2.724	2.572	0.0844	0.864
747.5	45.105	45.000	0.0583	0.597
765	90.100	90.000	0.0567	0.581
782.5	135.1	135.000	0.0567	0.581
799	177.45	177.420	0.0167	0.171

These results show an error magnitude near the bottom of the input range of between ½ and 1 V_{LSB}, and an error near the top of the range of between 0 and ½ LSB, indicating an effective resolution of around 9 bits.

4.2.4 Digital Decimator

The decimator was tested using Cadence ADE. Simulations were done to verify the functionality of the circuit. The behavior of the decimator should be that it outputs a 10-bit code on its 10 parallel output pins whose magnitude is proportional to the proportion of the input values that are high in a 10ms timespan. A new code should be output every 10ms.

The decimator's functionality was tested by connecting the output of the modulator to its input and observing the decimator's output codes with several input voltages applied to the modulator. Two output codes were collected at each voltage.

The results of this testing are given in Table 4.2.4.

Table 4.2.4: Decimator Simulation Results

Input Voltage (mV)	First Code	Second Code	Expected Code
730.068359375	3	2	1
752.5	257	256	256
765V	512	512	512
782.5	767	767	768
799.931640625	1023	1023	1023

These results show that the output code of the decimator with the modulator connected to its input varies by no more than two LSBs from the expected code.

4.3 Post-Fabrication Testing

Testing the physical IC after fabrication will require the use of a digital multimeter or oscilloscope to measure voltages, DC power supplies to provide bias voltages, an oven or dielectric bath to control chip temperature, and a computer with Excel to analyze the results of our measurements. We will also require anti-static wrist straps to avoid destroying our ICs through accidental electrostatic discharge. All this equipment is available to us in the labs in Coover Hall.

In addition to this standard lab equipment, we will also acquire a serial interface card that will allow the 10-bit parallel output of the ADC to be read by a computer. This card will be purchased from National Instruments for around $180. National Instruments also provides software that will read measured data from the card.

IEEE standards will be implemented during testing of the Delta Sigma data converter. The standard that will be used is the IEEE Standard for Terminology and Test Methods for Analog to Digital Converters[18]. This standard outlines testing methods that will allow us to characterize the data converter and determine the quality of its functionality. Following this standard will ensure that our testing results are accurate and that we use standard industry practices and reporting to allow the performance of our device to be easily compared to that of other ADCs.

4.3.1 Temperature Sensor

After fabrication, the temperature sensor will be tested with one of two methods. The first is with an oven in the VLSI lab in Coover Hall. The chip will be placed on a breadboard which will be placed in an oven. A multimeter probe will be connected to the temperature sensor's output pin through the porthole in the oven. The oven's temperature will then set to a variety of temperatures within the 10 to 60-degree Celsius range. At each temperature, the sensor's output voltage will be measured with the multimeter and recorded. These measurements will then be compared with the Cadence simulation results. If this testing method fails to give consistent results when taking measurements at the same temperature multiple times, the second method will be used.

The second method for testing the temperature sensor is to emerge the IC in an electrolytic bath. The bath consists of a vessel containing an electrolytic liquid which is heated to a well-controlled temperature. The output voltage will then be measured with a multimeter probe at a variety of temperatures.

4.3.2 ADC

After fabrication, the ADC's transfer characteristics will be tested using the lab equipment in the VLSI lab in Coover Hall and a serial interface card. DC power supplies will be used to provide the proper biasing voltages to the IC, and the serial interface card will be used to link the ADC's 10-bit parallel output to a computer to collect output data. The output of the temperature sensor will be connected to the input of the ADC, and we will use the known output voltage characteristics of the sensor to provide a variety of known voltages to the ADC by adjusting the temperature of the IC in an oven or dielectric bath as described in 4.3.1. The outputs from the ADC will be recorded for a variety of input voltages, and these measurements will be compared to those obtained through Cadence simulations. We will also use this data to extract a variety of characterization parameters for the ADC, such as monotonicity, differential nonlinearity, and integral nonlinearity.

In addition to obtaining the transfer characteristics of the ADC, we will also perform spectral characterization. We will do this by using the lab's function generator to apply a sinusoidal voltage signal to the ADC's input while using an oscilloscope to measure the harmonic distortion at the output. This will allow us to obtain the THD (Total Harmonic Distortion) and SNR (Signal to Noise Ratio) of the ADC.

4.4 Implementation and Testing Challenges

The primary challenges that we have and will face in the implementation and testing of our circuit are the short amount of time that we have available to build our circuit, and the long periods of time required to run Cadence simulations on our complete circuit.

Since our circuit design needs to be completed before the beginning of June so that we can have it fabricated over the summer, we have had only one semester to complete the research, design, and computer simulation stages of our project. This has required us to spend a significant amount of our already scarce time this semester on these stages.

The long periods of time that it takes to run Cadence simulations on our complete circuit has made it difficult to test the effects of small changes on the performance of our complete circuit. One way we have mitigated the effects of this problem by testing only one segment of our circuit at a time to measure its performance as its design is being improved. This allows simulations to run more quickly because fewer circuit nodes need to have calculations done for them. Another way we have mitigated the effects of this problem are by running simulations using ideal clock sources rather than the clock that we built. This

allows for a significant reduction in simulation time due to the elimination of the need to perform large numbers of calculations on the nodes of the ring oscillator in the clock.

One challenge that we foresee for the future is in using the temperature sensor to test the ADC after fabrication. Changing the temperature of a circuit can affect the way that the transistors operate. Since the temperature sensor and ADC will be on the same chip, the ADC's temperature will be different for measuring different inputs from the temperature sensor. The effect of these temperature differences on the ADC could introduce some nonlinearity in our testing results.

4.5 Nonfunctional Requirements

The preceding sections of Part 4 have discussed implementation and testing for the functional requirements of our project, which are all but one of the requirements. The only non-functional requirement is that the circuit layout dimensions not exceed 4 millimeters by 4 millimeters. As can be seen from the figures in section 3.7, our final circuit layout has dimensions of [[[**ADD**]]]. This is much smaller than our allowed area, which will allow our ADC to be integrated in other ICs without consuming a significant amount of die space.

5 Closing Material

5.1 Closing Summary

The goal of our project was to design a high-resolution data converter IC that converts analog voltage to a digital representation. The data converter is implemented along with a temperature sensor in a single chip to allow the chip's temperature to be communicated as a digital signal. The accurate high-resolution measurement can then be used to trigger the chip to throttle its operation to prevent overheating. After researching ADC architectures, we decided to use a specific delta-sigma ADC architecture to realize our IC for its high accuracy, low power consumption, and simplicity. Our IC has 10-bits of resolution and measures a temperature range from 10C to 60C with an oversampling ratio of 1024 to 1, which means that for every 1024 samples taken at the input, one sample will be asserted at the output. The delta-sigma ADC is comprised of several functional blocks. All these components are designed at the transistor level, and tested individually and combined, to make sure that the product will be functional after fabrication.

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